Sandia National Laboratories

IMMERSION COOLING OF POWER ELECTRONICS

ADVANCED PACKAGING

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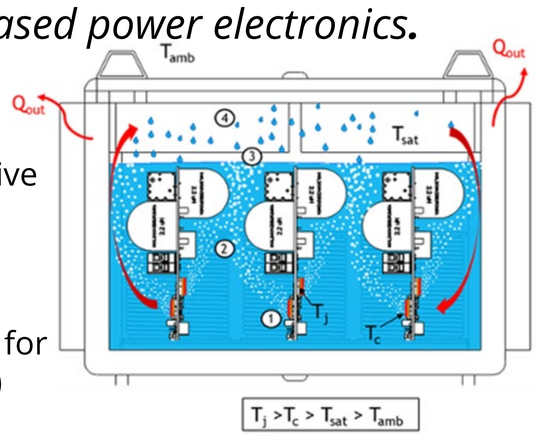
OBJECTIVES

Develop an all encompassing, completely passive cooling solution for grid-level energy storage-based power electronics.

Primary Objectives

- ***Model*** candidate non-electrically conductive engineered fluids using advanced Finite Element Method boiling models (FY25)
- ***Develop*** a double-side cooled, flip-chip package with integrated finned heatsinks for the power semiconductor switches (FY26)
- ***Design & fabricate*** a 1 kW two-phase immersion cooling solution exemplar (FY27)



Conceptual schematic of proposed cooling solution

BACKGROUND

- Current immersion cooling used in advanced data centers utilize external heat exchanger and ***pumped liquid cooling loop*** to enable high power density (2-5 kW/m^3).
- This method not directly applicable to grid integration since it:
  - Requires ***significant maintenance*** to ensure maximum performance.
  - ***Lowers system lifetime*** due to actively pumped thermal loop
- Previous Sandia-funded Laboratory Directed Research and Development project (#224288) developed preliminary tools and analysis for ”system-as-a-heat pipe” concept
  - Correlations between critical heat flux, system pressure, and MOSFET junction temperature were developed

HYPOTHESIS, MOTIVATION, & IMPACT

To be implemented in remote areas that have harsh environmental conditions (e.g., New Mexico), Energy Storage Systems require very long (20 year) lifetimes, zero maintenance, and very low operational-costs.

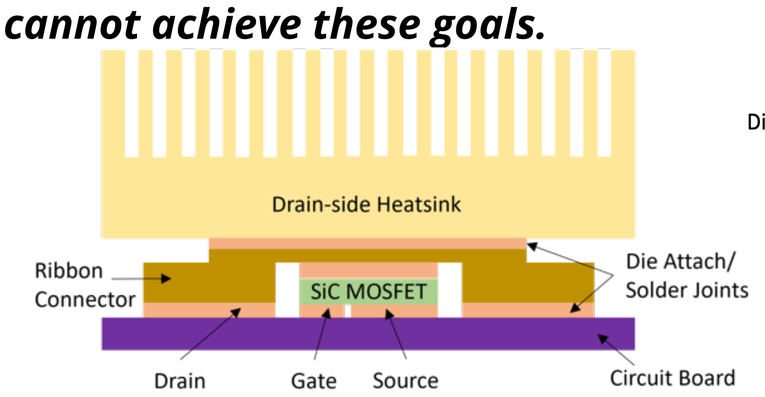
Typical Active Cooling methods (forced air/liquid) cannot achieve these goals.

Hypothesis

- Removal of heat exchanger and cooling loop while maintaining sufficient heat flux would ***enable significantly more robust, cost-effective thermal management*** for energy storage-based power electronics

Packaging Innovation

- Passive immersion cooling system requires double-side cooled, flip-chip package with integrated heatsinks for the power semiconductor switches.
- Package will maximize thermal dissipation with optimized size/layout of heatsink fins as determined by FEM models



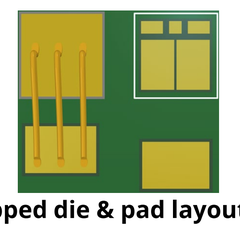
Schematic of single-side cooled, flip-chipped MOSFET and integrated fin heatsink

METHODOLOGY & TESTING

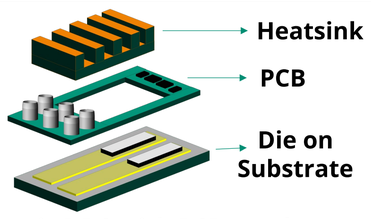
Design

Develop in-house processes for flip chip bonding (FY25)

- Direct die-on-PCB
- Die on Direct Bond Copper (DBC) substrate



Flipped die & pad layout



Ceramic DBC with PCB overlay

Fabricate

Single-side cooled package (FY25)

Double-side cooled package (FY26)

Optimized heatsink (FY26)

Flip-chip die bonder

Wire bonder

Reflow Oven

3D Printer

CNC Mill

In-house capabilities

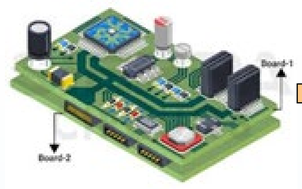
HEATSINKUSA
American Made Since 2009

American Standard Circuits
Sunstone Circuits

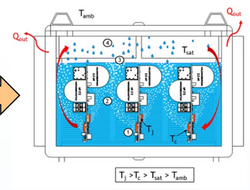
Commercial

Integrate

Double-side cooled module inserted into 1kW immersion cooled prototype (FY27)



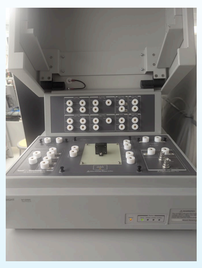
PCB-based assembly

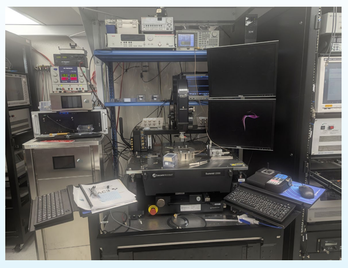


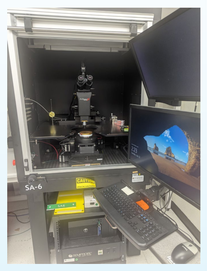
Assembly in 1 kW prototype

Evaluate

Electro-thermal Performance benchmark to active cooling (FY27)



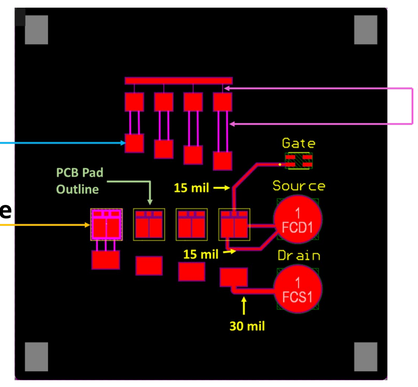


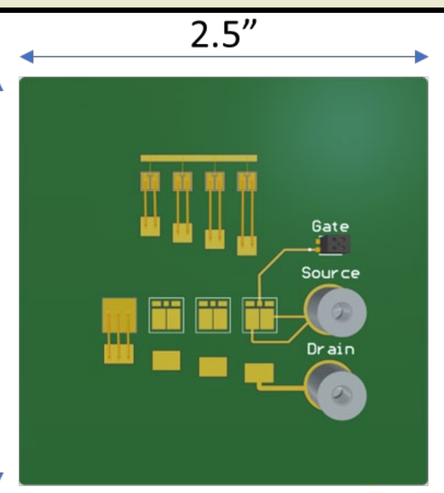


RESULTS

Process development PCB

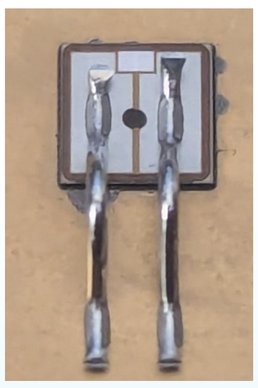
Schematic of double-side cooled package

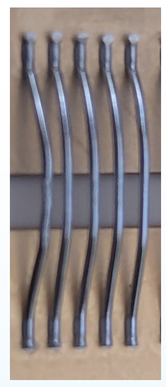


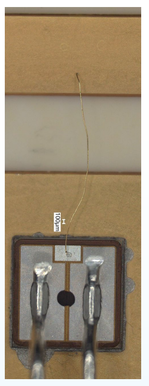


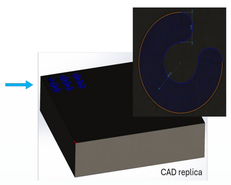
1. Determine process parameters for die and wire bonding on PCB
2. Evaluate electrical performance of flip-chipped die on board

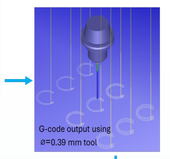
Fabrication procedures

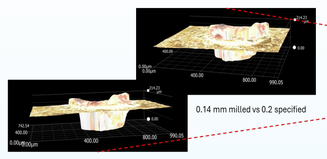


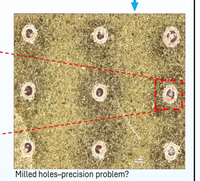












Initial results

1. Die attach, heavy-gauge wire, uniform array, and fine wire processes developed for DBC
2. DBC mounting on Al-block, G-code generation, hole array investigation for accuracy/uniformity of in-house manufacturing of custom DBCs

U.S. DEPARTMENT of ENERGY
National Nuclear Security Administration

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