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HAFNIA GATE DIELECTRICS FOR ENERGY CONVERSION

Presentation ID 805

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FROM ENERGY STORAGE SYSTEMS TO GATE DIELECTRICS

1. ENERGY STORAGE SYSTEM

Stores energy ...
(DC electricity)

Energy storage systems rely on efficient power conversion to deliver electricity to the grid or end users.

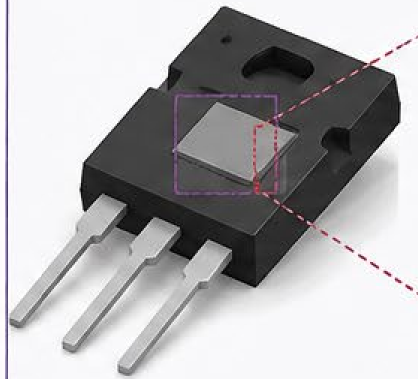
2. POWER CONVERSION SYSTEM

Converts and controls power ...
(DC ↔ AC, regulate voltage, frequency, power flow)

Power electronics modules use semiconductor switches to efficiently convert and control power.

3. POWER SEMICONDUCTOR DEVICE

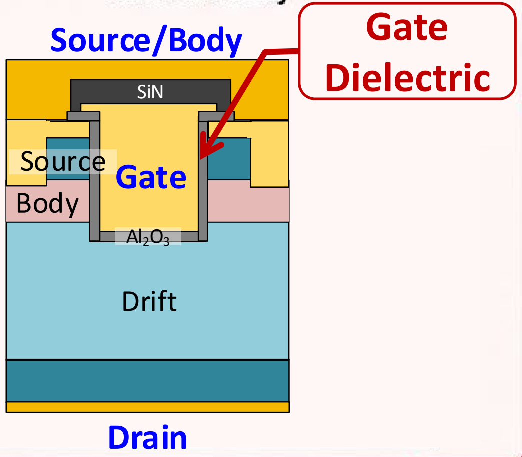
Performs fast, efficient switching ...
(heart of power conversion)



Wide bandgap devices (SiC, GaN) enable higher voltage, lower losses, and higher efficiency.

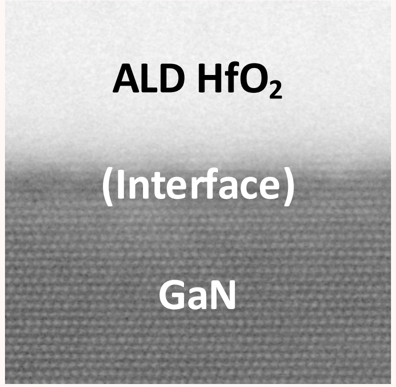
4. GATE DIELECTRIC (KEY ENABLER)

Enables voltage control with high performance and reliability



The gate dielectric is a thin insulating layer that:

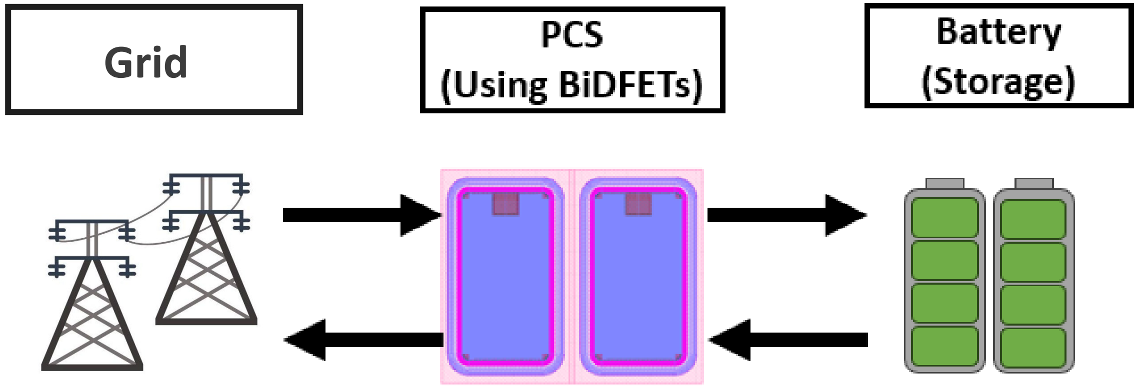
- ✓ Controls the channel with the gate voltage
- ✓ Impacts channel resistance (R_{ch})
- ✓ Affects switching speed, losses, and efficiency
- ✓ Determines reliability and lifetime

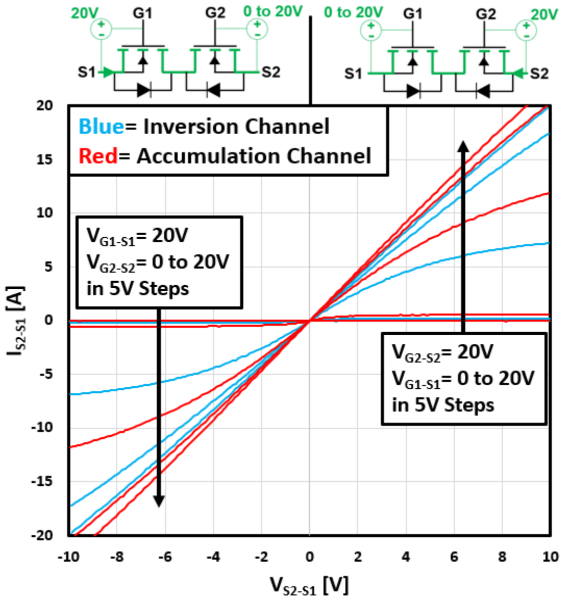


Improving the gate dielectric enables lower losses, higher efficiency, greater reliability, and reduced system cost—driving better performance for energy storage and the electric grid.

SIC POWER SEMICONDUCTORS UNDER ENERGY STORAGE: 2022-2024

"Power conversion systems are an enabling technology for energy storage systems."





Goal:

Develop semiconductors to enable advancements in power conversion systems

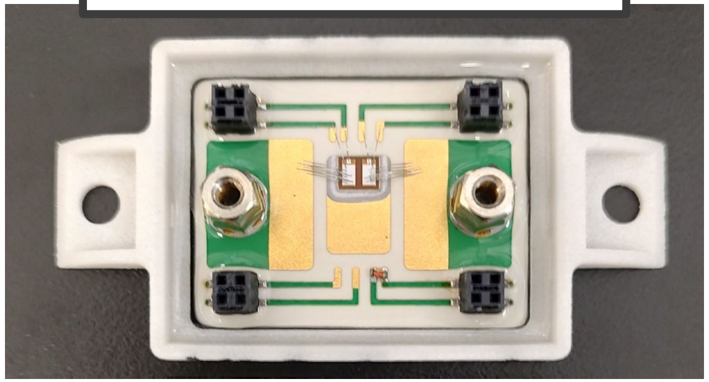
Total funding: **$1M**
Duration: **2 years**

Key Partnerships:

University at Albany, State University of New York
NoMIS Power
The Ohio State University

Worlds first > 3kV monolithic SiC BiDFET

Monolithically Integrated BiDFET Package



FUNDAMENTAL CHALLENGE BELOW 3300 V

Image courtesy of Woongje Sung

1

SiC and GaN have a tremendous performance advantage over Si

Unipolar Figure-of-Merit (UFOM)

Fundamental limit-line

2

Practically, results diverge from limit-line at 1700 V and below

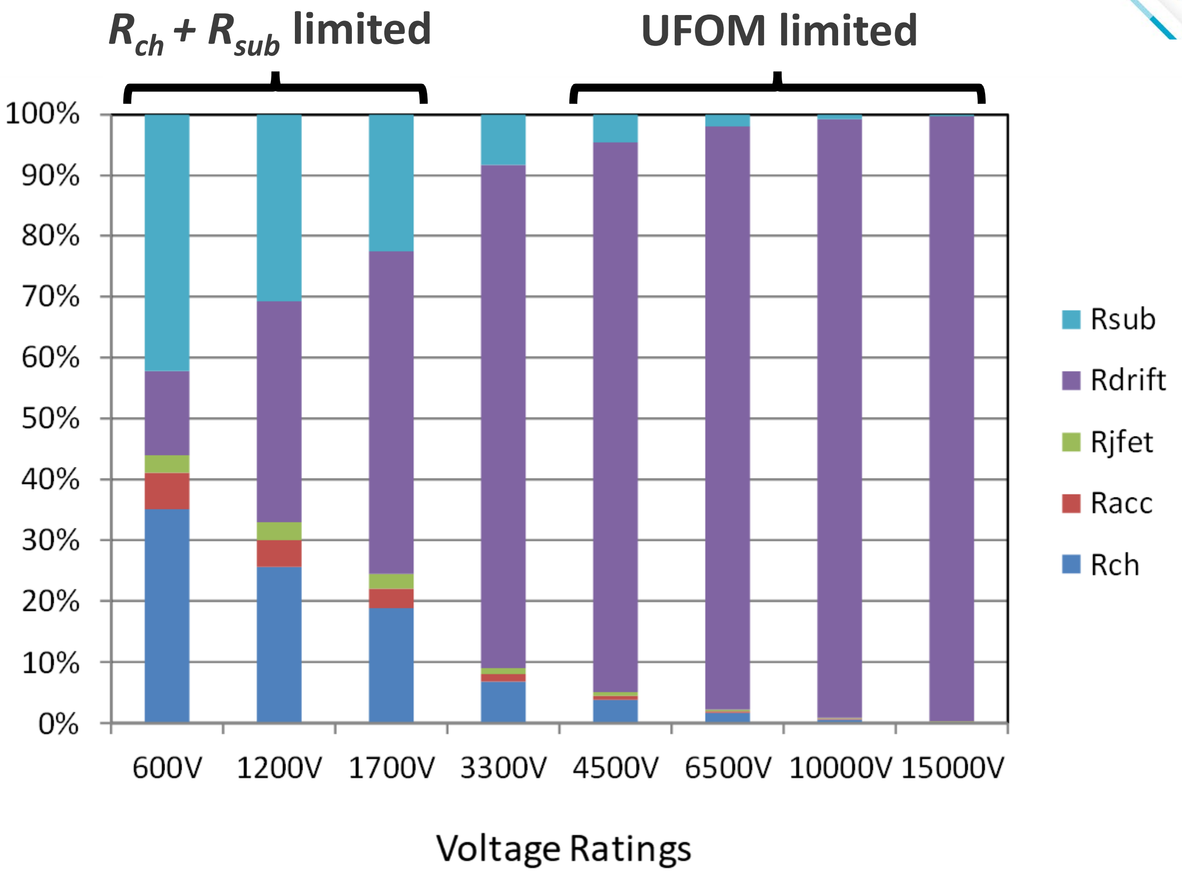
3

Significant performance loss to channel and substrate resistance

4

Improvements to R_{ch} and R_{sub} could improve performance by **60-75%**

SiC DMOS $R_{on,sp}$ Example



High-k (high permittivity)

ε: 3.9 → 25

6×

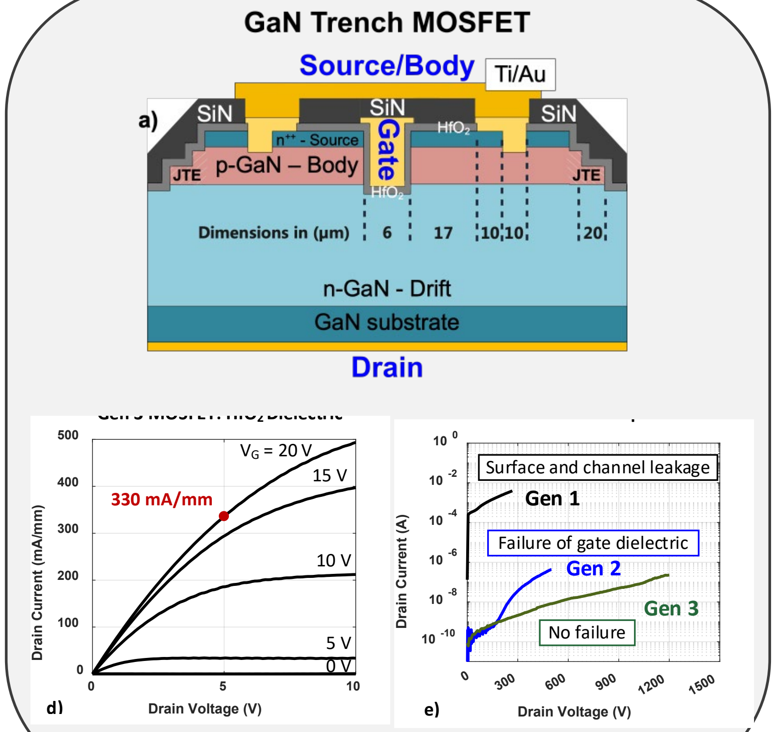
$$R_{ch,sp} \propto \frac{1}{\mu_N \cdot \boldsymbol{\varepsilon}/d}$$

≈ 25 ×

SANDIA'S GAN MOSFET: HAFNIA ON GAN

Worlds 1st

1.2 kV HfO_2-Gated GaN Trench MOSFET



On-state current density of **330 mA/mm** at V_D = 5V

- **> 10×** improvement compared to highest known reports

Near-commercial 1.2 kV, 3.75 mΩ-cm^2 **SiC D-MOSFETs** measured at **27 mA/mm**

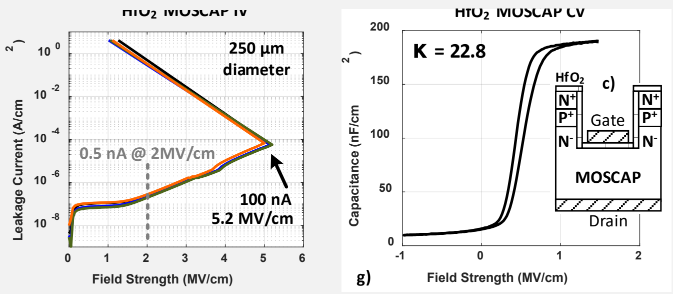
Other vGaN MOSFETs report 25 mA/mm

Estimated that with 10 µm cell pitch this translates to **1.1 mΩ-cm^2**

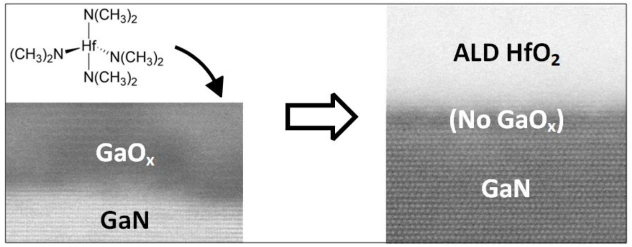
Enabled by:

Worlds 1st

HfO_2 Gate Dielectric for vGaN



Interface Conversion Process



First demonstration of HfO_2 on GaN with simultaneous:

1. Low leakage current
2. High breakdown strength
3. High dielectric constant

Funded by: DOE Transportation Technologies Office

A. T. Binder *et al* 2024 *Appl. Phys. Express* **17** 101003

TRANSFERRING THE TECHNOLOGY TO SIC

DOE-OE funding exposed the bottleneck.

DOE-TTO hafnia work solved part of it in GaN.

That insight motivated transferring hafnia back into SiC.

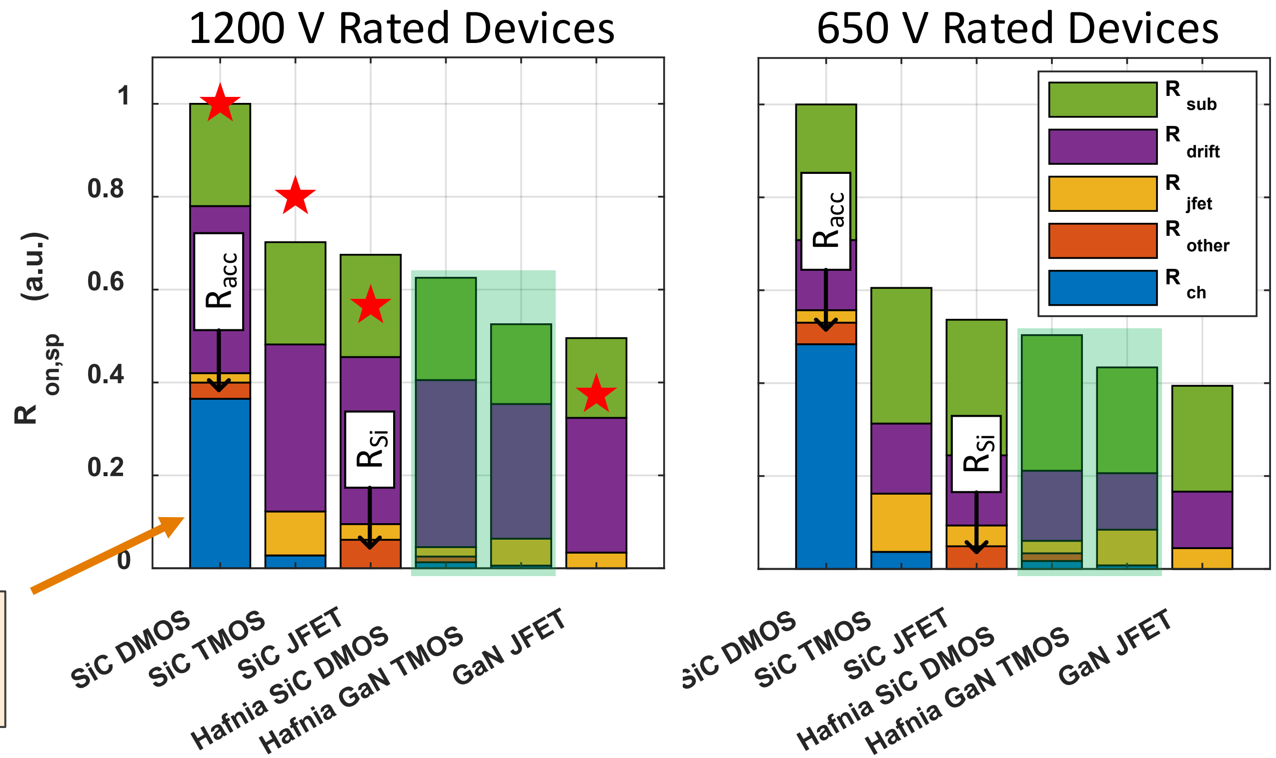
Capability to enhance performance and reliability (including extreme operating conditions)

Potential for DMOS to perform equal to TMOS

Why SiC?

- Robust foundry ecosystem already in place
- Higher TRL for SiC compared to GaN
  - Quick impact to real systems
  - Quick to deploy once proven

Minimize R_{ch} through high-k gate dielectric



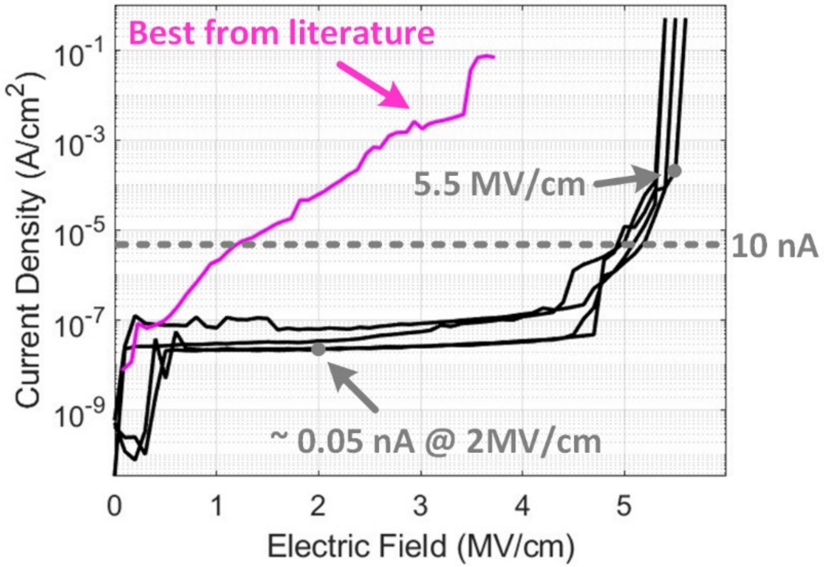
POTENTIAL FOR HfO_2 AND HIGH-K ON SILICON CARBIDE

2025 R&D 100 WINNER

Sandia's bulk HfO_2-on-SiC

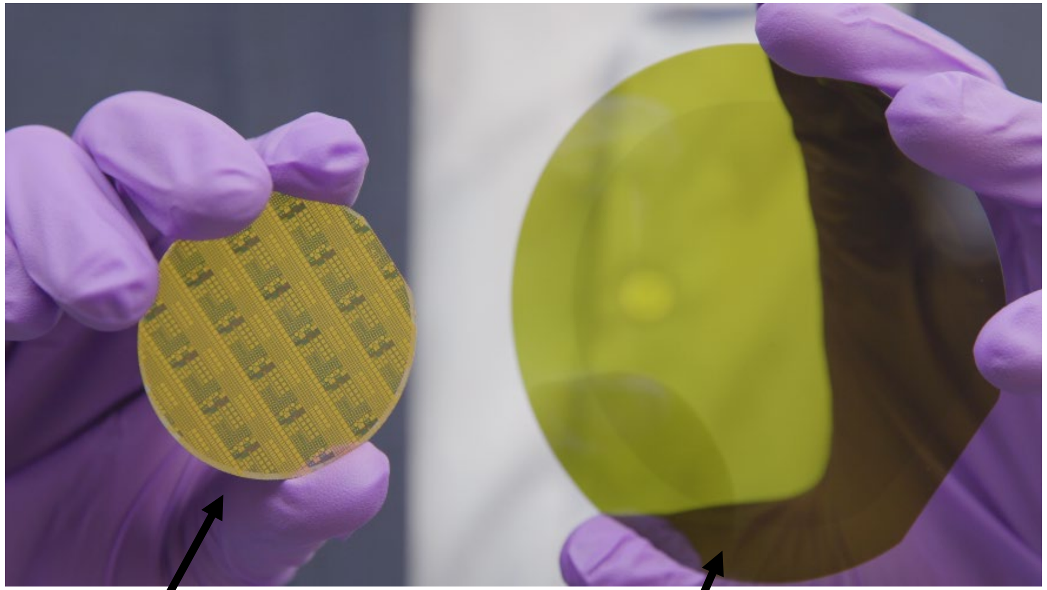
Demonstrated record setting static performance of HfO_2 on SiC

HfO_2-on-SiC MOSCAP IV



Appl. Phys. Lett. 92, 042904 (2008)

Four orders of magnitude reduction in leakage at driving strength (2 MV/cm)



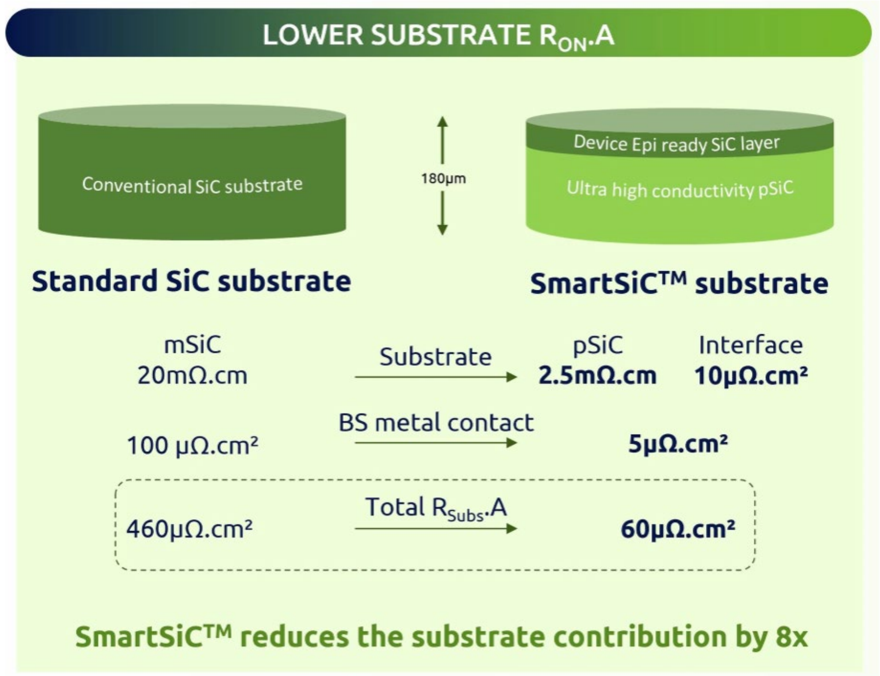
Hafnia-gated GaN MOSFETs

Hafnia film sample on 4" SiC

HfO_2 is capable for SiC as well as GaN

Minimize R_{ch} through high-k gate dielectric

FUTURE OF WBG: SUMMARY

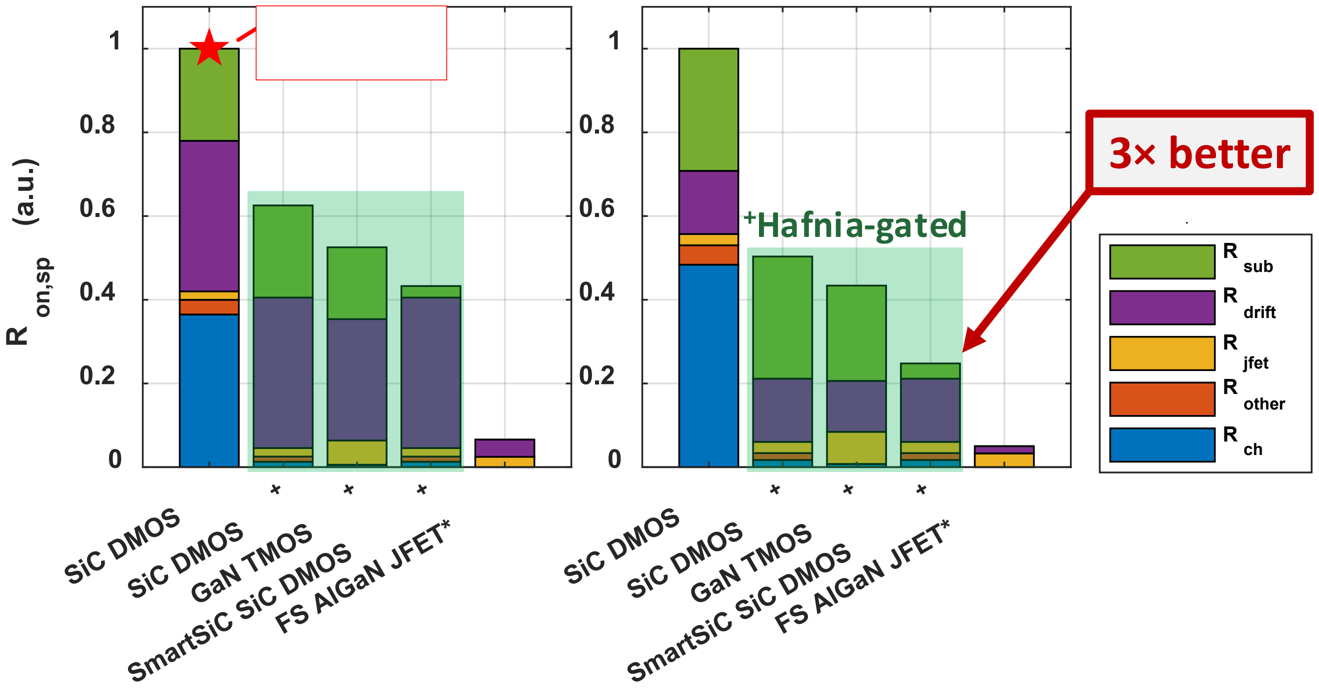


Soitec presentation, first shown at CS International in Brussels 2023

Tremendous potential for unrealized gains in 650-1700 V devices

2-3× improvement over present state-of-the-art

Next generation high-k gate dielectrics
Substrate technology

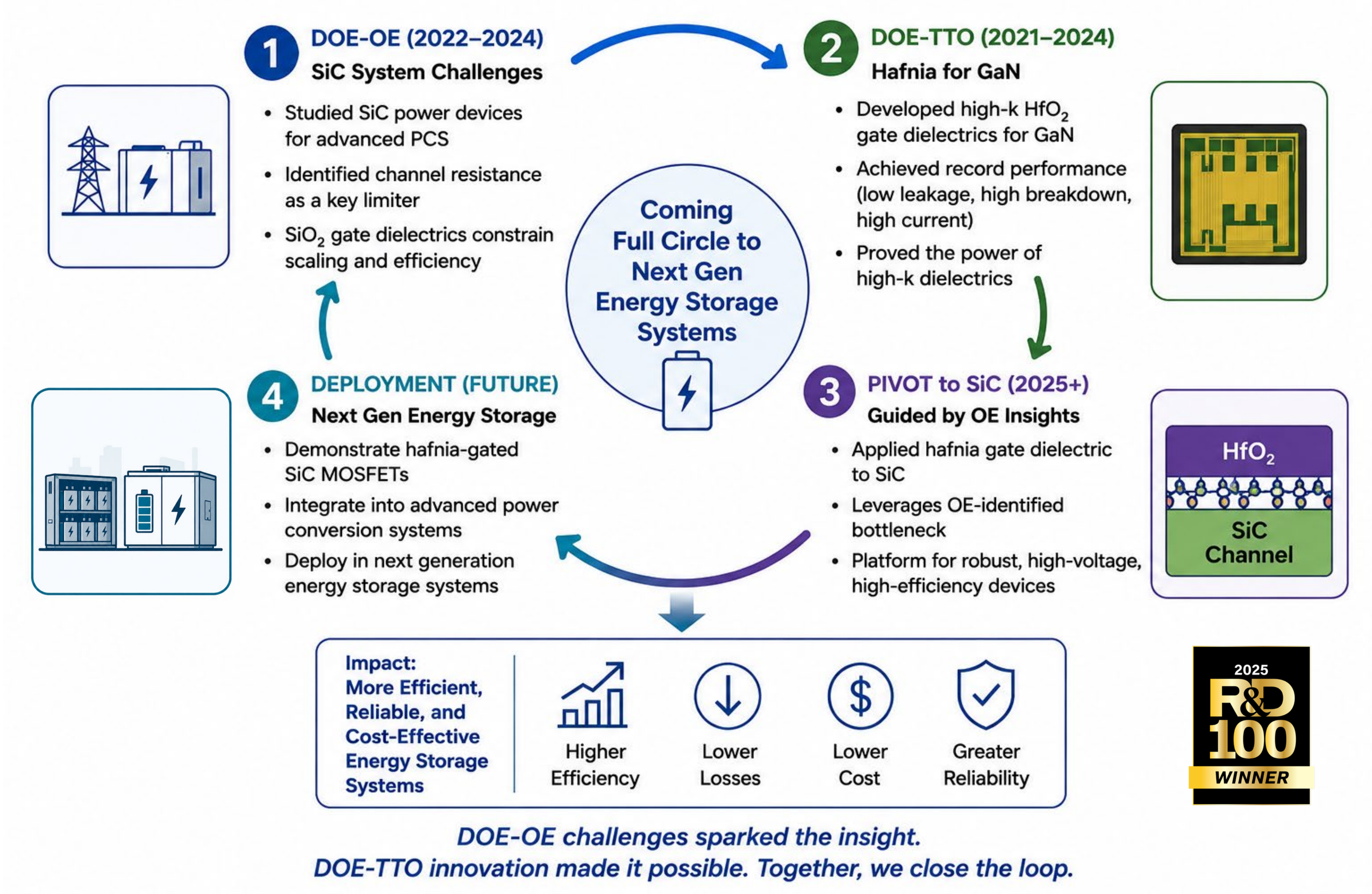


Poly-SiC wafers can reduce cost and further improve R_{on}

Will be available at X-FAB

Announced: May 22, 2024

FULL CIRCLE: FROM DOE-OE SIC CHALLENGES TO NEXT GEN. ENERGY STORAGE



Questions?

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